



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T373-1600-36

Mean on-state current	I_{TAV}		1600 A	
Repetitive peak off-state voltage	V_{DRM}		3000 ÷ 3600 V	
Repetitive peak reverse voltage	V_{RRM}			
Turn-off time	t_q		500, 630, 800 μ s	
V_{DRM}, V_{RRM}, V	3000	3200	3400	3600
Voltage code	30	32	34	36
$T_j, ^\circ C$	-60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	1600 1855	$T_c=92^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	2512	$T_c=92^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	36.0 41.0	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			38.0 44.0	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	6480 8405	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			5990 8030	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000 ÷ 3600	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100 ÷ 3700	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; single pulse; Gate open
V_{D}, V_R	Direct off-state and Direct reverse voltages	V	0.75· V_{DRM} 0.75· V_{RRM}	$T_j=T_{j\ max}$; Gate open

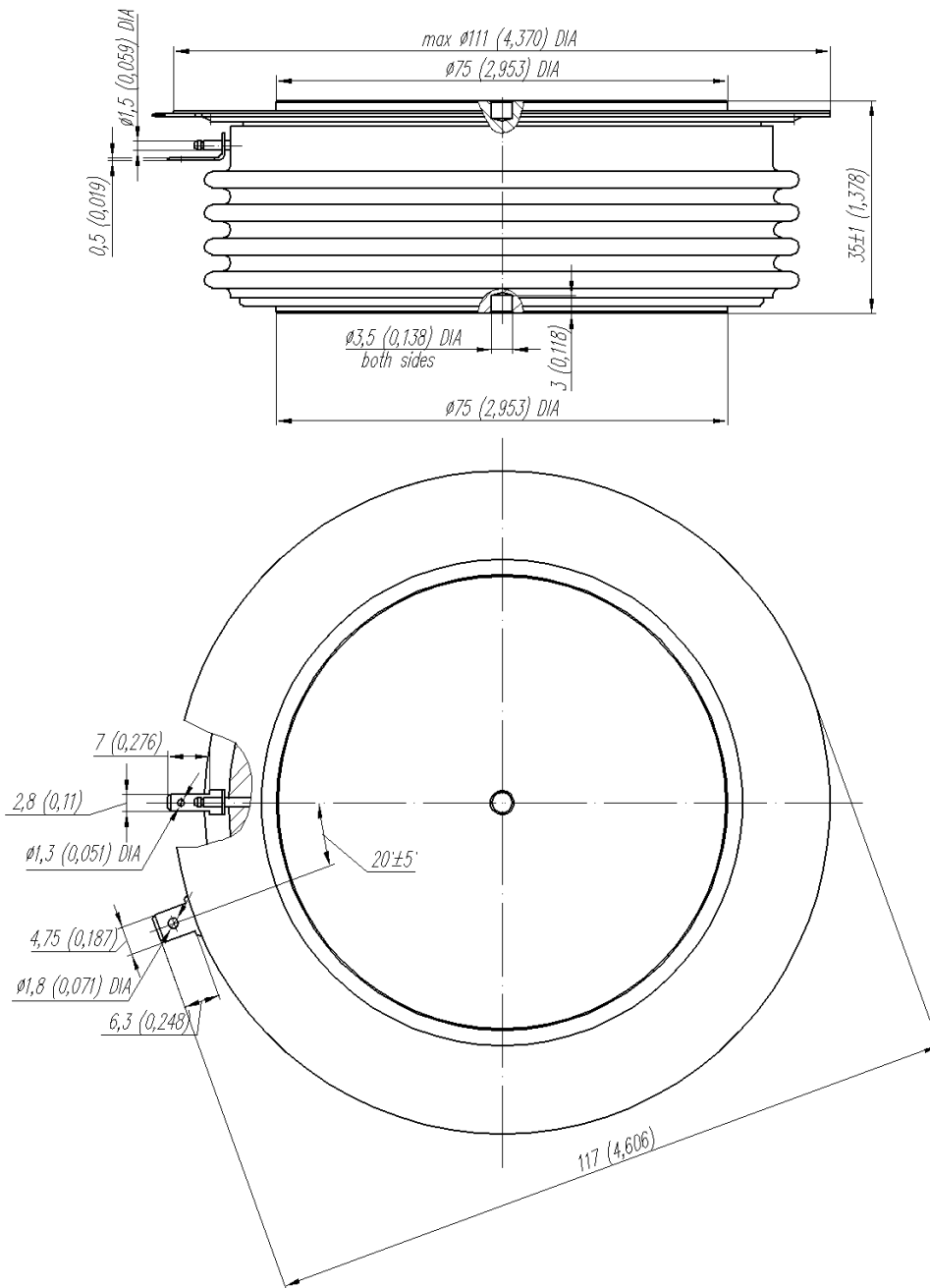
TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	800	$T_j = T_{j\ max}; V_D = 0.67 \cdot V_{DRM}; I_{TM} = 2 I_{TAV};$ Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60÷50	
T_j	Operating junction temperature	$^{\circ}$ C	-60÷125	
MECHANICAL				
F	Mounting force	kN	40.0÷50.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.05	$T_j = 25 \text{ }^{\circ}\text{C}; I_{TM} = 5024$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.15	$T_j = T_{j\ max};$	
r_T	On-state slope resistance, max	m Ω	0.220	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25 \text{ }^{\circ}\text{C};$ $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j = T_{j\ max};$ $V_D = V_{DRM}; V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$ Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}\text{C}$ $T_j = T_{j\ max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			3.00		
			2.00		
I_{GT}	Gate trigger direct current, max	mA	500	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}\text{C}$ $T_j = T_{j\ max}$	
			300		
			200		
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$	
I_{GD}	Gate non-trigger direct current, min	mA	15.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	3.00	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 0.4 \cdot V_{DRM}; I_{TM} = I_{TAV};$ Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 2$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	500, 630, 800	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}; I_{TM} = I_{TAV};$ $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.010	Direct current	Double side cooled
R_{thjc-A}			0.022		Anode side cooled
R_{thjc-K}			0.018		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.002	Direct current	
MECHANICAL					
w	Weight, typ	g	1600		
D_s	Surface creepage distance	mm (inch)	55.13 (2.170)		
D_a	Air strike distance	mm (inch)	25.10 (0.988)		

PART NUMBERING GUIDE							NOTES													
T	373	1600	36	A2	E2	N														
1	2	3	4	5	6	7														
1. Phase Control Thyristor 2. Design version 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of on-state current non-repetitive, V/μs 6. Turn-off time (dv _D /dt=50 V/μs) 7. Ambient conditions: N – normal; T – tropical							1) Critical rate of rise of on-state current non-repetitive <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Symbol of Group</th> <th>P2</th> <th>K2</th> <th>E2</th> <th>A2</th> </tr> </thead> <tbody> <tr> <td>(dv_D/dt)_{crit}, V/μs</td> <td>200</td> <td>320</td> <td>500</td> <td>1000</td> </tr> </tbody> </table>				Symbol of Group	P2	K2	E2	A2	(dv _D /dt) _{crit} , V/μs	200	320	500	1000
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All dimensions in millimeters (inches)

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