



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T333-320-28

Mean on-state current		I_{TAV}		320 A	
Repetitive peak off-state voltage		V_{DRM}		2000 ÷ 2800 V	
Repetitive peak reverse voltage		V_{RRM}			
Turn-off time		t_q		200, 250, 320, 400, 500 μ s	
V_{DRM}, V_{RRM}, V	2000	2200	2400	2600	2800
Voltage code	20	22	24	26	28
$T_j, ^\circ C$	-60 ÷ 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	320 388	$T_c=95^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	502	$T_c=95^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	6.5 7.5	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			6.8 7.8	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	211 279	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			193 256	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000 ÷ 2800	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100 ÷ 2900	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75 \cdot V_{DRM}$ $0.75 \cdot V_{RRM}$	$T_j=T_{j\ max}$; Gate open

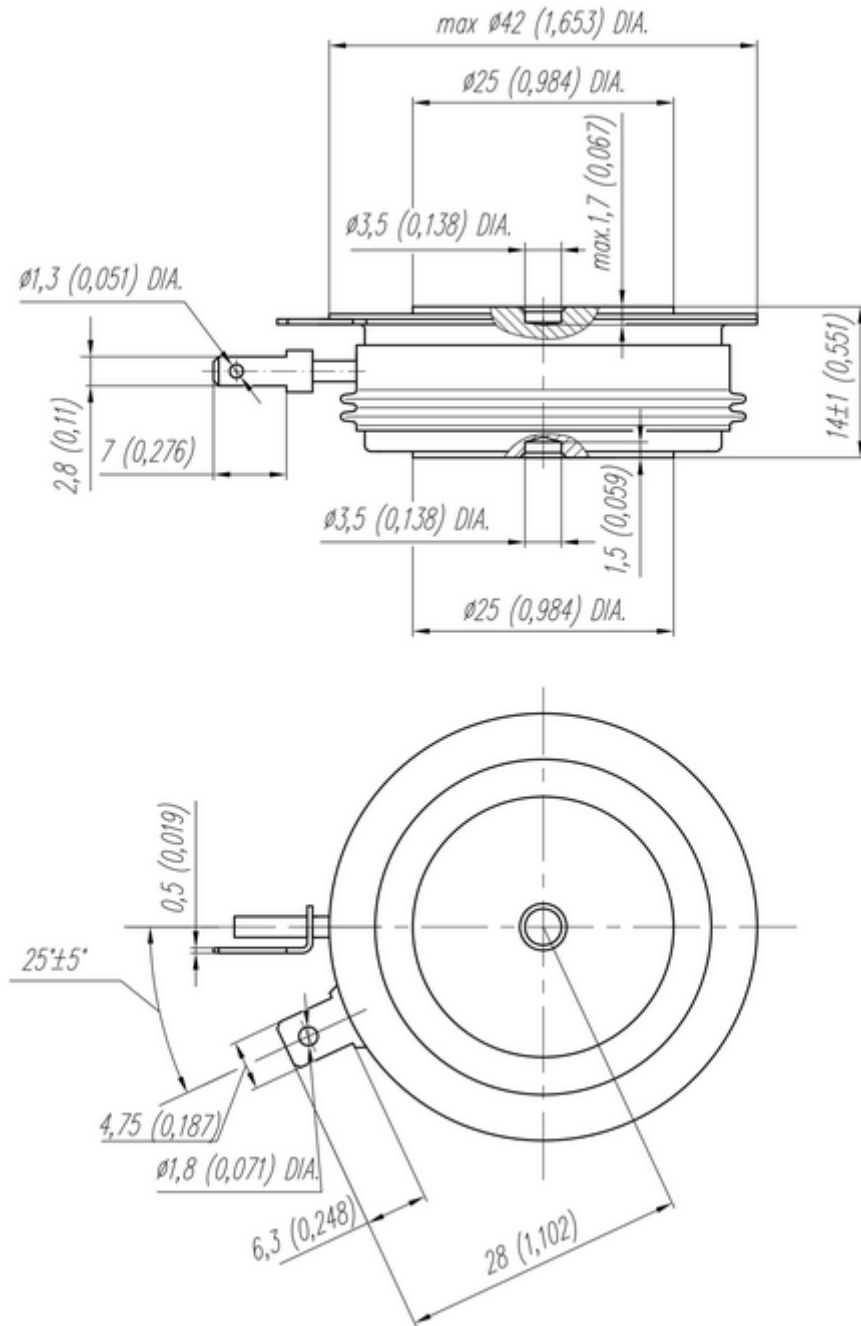
TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	320	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2 I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60÷50	
T_j	Operating junction temperature	$^{\circ}$ C	-60÷125	
MECHANICAL				
F	Mounting force	kN	9.0÷11.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.10	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 1005$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.15	$T_j = T_{j\ max}$;	
r_T	On-state slope resistance, max	$m\Omega$	1.500	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	700	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j = T_{j\ max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00	$T_j = T_{j\ min}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			2.50	$T_j = 25$ $^{\circ}$ C	
			2.00	$T_j = T_{j\ max}$	
I_{GT}	Gate trigger direct current, max	mA	400	$T_j = T_{j\ min}$	
			250	$T_j = 25$ $^{\circ}$ C	
			200	$T_j = T_{j\ max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	10.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	2.50	$T_j = 25$ $^{\circ}$ C; $V_D = 0.4 \cdot V_{DRM}$; $I_{TM} = I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 2$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	200, 250, 320, 400, 500	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.040	Direct current	Double side cooled
R_{thjc-A}			0.088		Anode side cooled
R_{thjc-K}			0.072		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.008	Direct current	
MECHANICAL					
w	Weight, typ	g	110		
D_s	Surface creepage distance	mm (inch)	10.30 (0.405)		
D_a	Air strike distance	mm (inch)	6.30 (0.248)		

PART NUMBERING GUIDE							NOTES																
T	333	320	28	A2	P2	N	1) Critical rate of rise of on-state current non-repetitive																
1	2	3	4	5	6	7	<table border="1"> <thead> <tr> <th>Symbol of Group</th> <th>P2</th> <th>K2</th> <th>E2</th> <th>A2</th> </tr> </thead> <tbody> <tr> <td>$(dv_D/dt)_{crit}, V/\mu s$</td> <td>200</td> <td>320</td> <td>500</td> <td>1000</td> </tr> </tbody> </table>					Symbol of Group	P2	K2	E2	A2	$(dv_D/dt)_{crit}, V/\mu s$	200	320	500	1000		
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$t_q, \mu s$	200	250	320	400	500																		
3. Mean on-state current, A																							
4. Voltage code																							
5. Critical rate of rise of on-state current non-repetitive, $V/\mu s$																							
6. Turn-off time ($dv_D/dt=50 V/\mu s$)																							
7. Ambient conditions: N – normal; T – tropical																							



All dimensions in millimeters (inches)