



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T273-3200-18

Mean on-state current	I_{TAV}	3200 A
Repetitive peak off-state voltage	V_{DRM}	1600 ÷ 1800 V
Repetitive peak reverse voltage	V_{RRM}	
Turn-off time	t_q	250 μ s
V_{DRM}, V_{RRM}, V	1600	1800
Voltage code	16	18
$T_j, ^\circ C$	-60 ÷ 125	

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	3200	$T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	5024	
I_{TSM}	Surge on-state current	kA	57.0 66.0	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			60.0 69.0	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	16245 21780	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			14940 19755	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1600 ÷ 1800	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1700 ÷ 1900	$T_{j\ min} < T_j < T_{j\ max}$; 180° half-sine wave; 50 Hz; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75 \cdot V_{DRM}$ $0.75 \cdot V_{RRM}$	$T_j=T_{j\ max}$; Gate open

TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	630	$T_j = T_{j\ max}; V_D = 0.67 \cdot V_{DRM}; I_{TM} = 2 I_{TAV};$ Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 ÷ 125	
T_j	Operating junction temperature	$^{\circ}$ C	-60 ÷ 125	
MECHANICAL				
F	Mounting force	kN	40.0 ÷ 50.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

CHARACTERISTICS

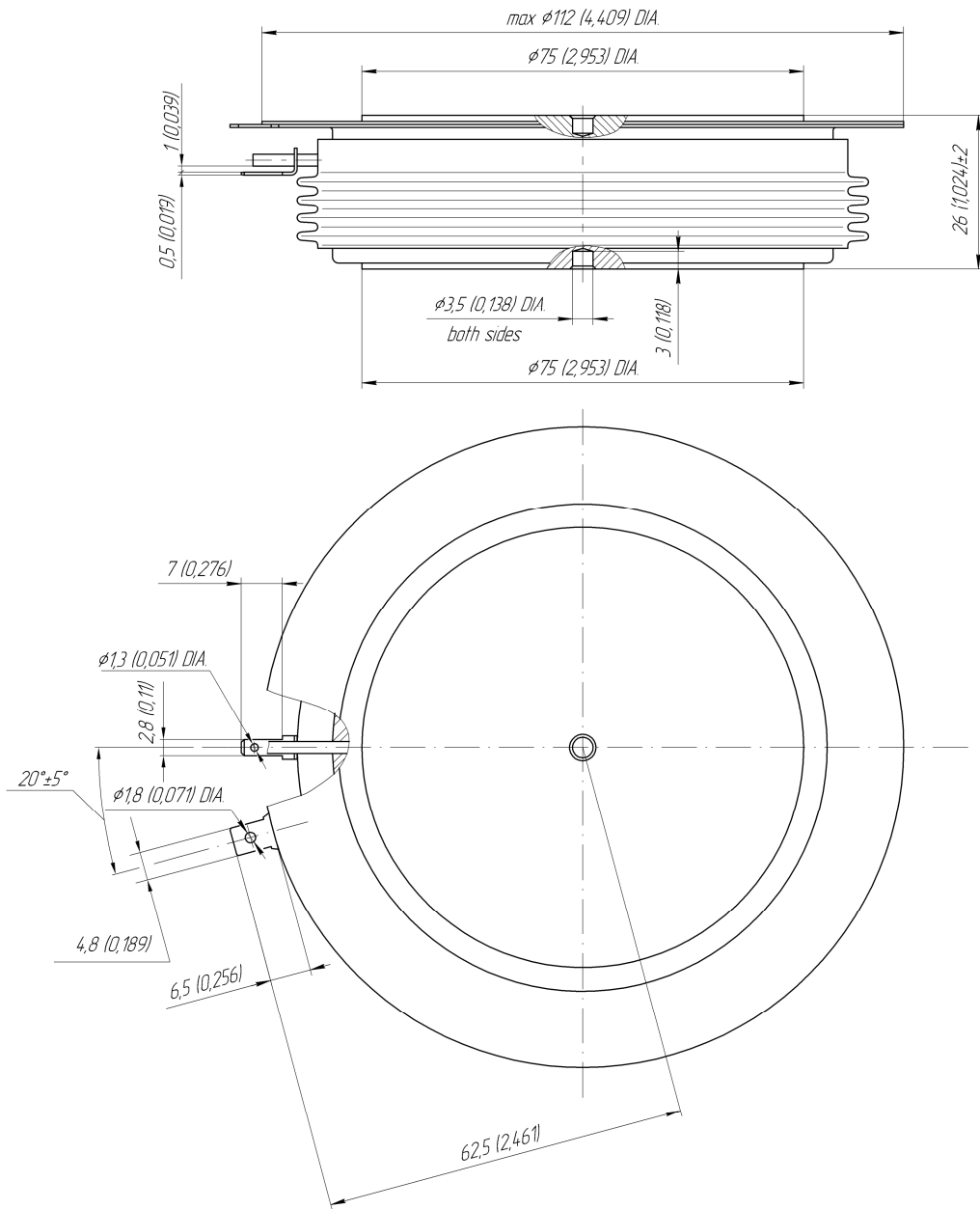
Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.45	$T_j = 25 \text{ }^{\circ}\text{C}; I_{TM} = 7850$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.81	$T_j = T_{j\ max};$	
r_T	On-state slope resistance, max	m Ω	0.084	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25 \text{ }^{\circ}\text{C};$ $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j = T_{j\ max};$ $V_D = V_{DRM}; V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	1000	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$ Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}\text{C}$	Direct gate current
			3.00		
I_{GT}	Gate trigger direct current, max	mA	500	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}\text{C}$	
			300		
V_{GD}	Gate non-trigger direct voltage, min	V	2.00	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$	
			0.35		
I_{GD}	Gate non-trigger direct current, min	mA	15.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	2.00	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 0.4 \cdot V_{DRM}; I_{TM} = 2000$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	250	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}; I_{TM} = 2000$ A; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	
Q_{rr}	Total recovered charge, max	μ C	4200	$T_j = T_{j\ max}; I_{TM} = 2000$ A;	
t_{rr}	Reverse recovery time, max	μ s	38	$di_R/dt = -10$ A/ μ s;	
I_{rrM}	Peak reverse recovery current, max	A	221	$V_R = 100$ V	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0085	Direct current	Double side cooled
R_{thjc-A}			0.0187		Anode side cooled
R_{thjc-K}			0.0153		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0020	Direct current	
MECHANICAL					
w	Weight, typ	g	1500		
D_s	Surface creepage distance	mm (inch)	36.60 (1.441)		
D_a	Air strike distance	mm (inch)	16.20 (0.638)		

PART NUMBERING GUIDE

T	273	3200	18	N
1	2	3	4	5

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Ambient conditions: N – normal; T – tropical



All dimensions in millimeters (inches)

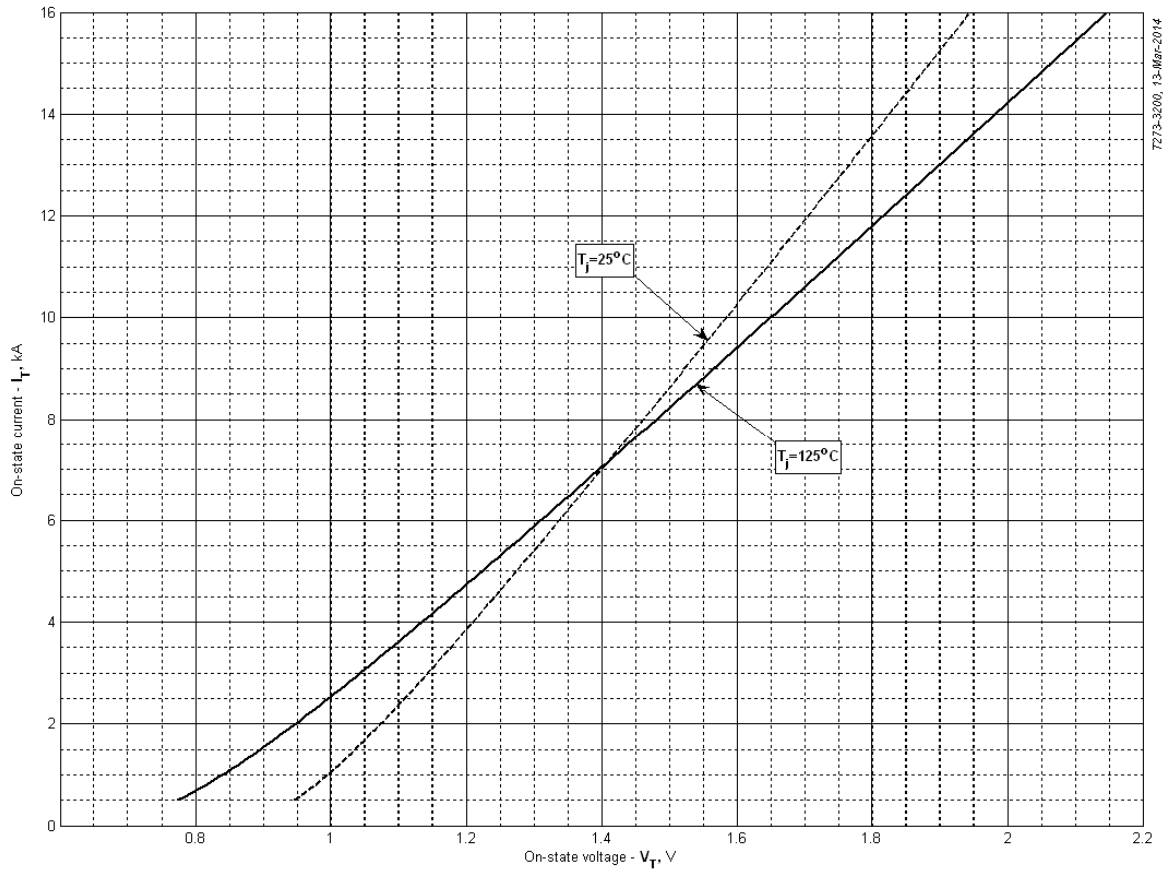


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	$T_j = 25^\circ\text{C}$	$T_j = T_{j\text{max}}$
A	0.950448	0.778423
B	0.067399	0.092520
C	0.164566	0.219790
D	-0.137520	-0.183667

On-state characteristic model (see Fig. 1)

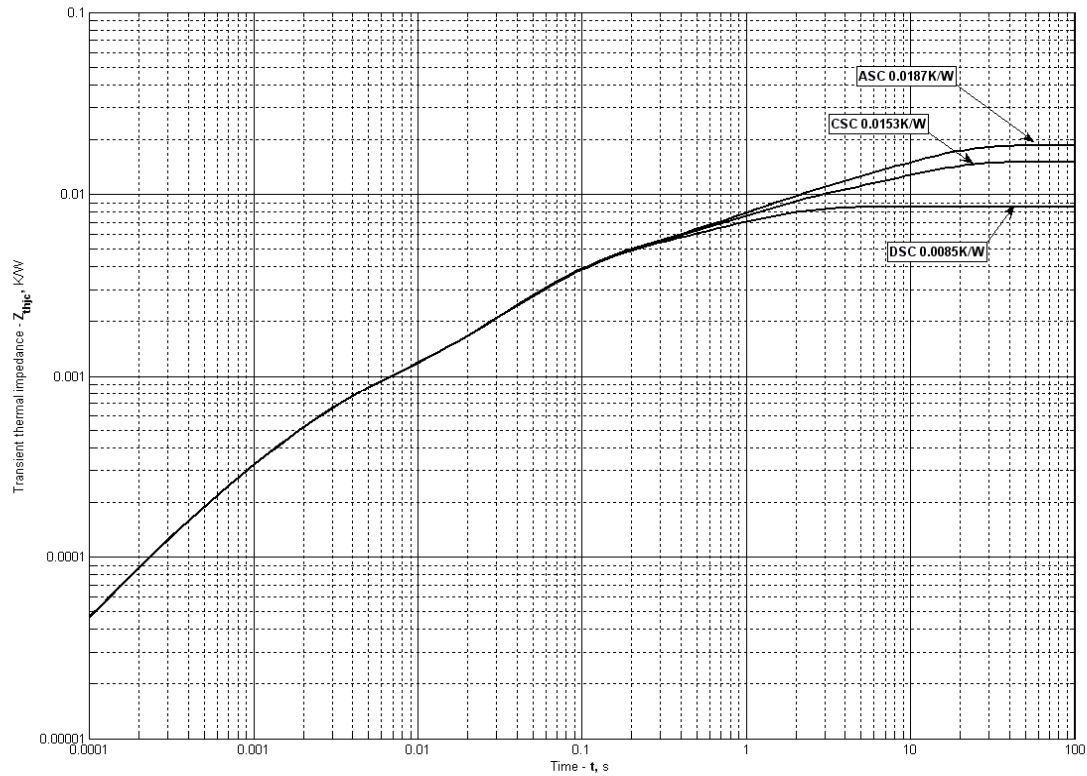


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^n R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where $i = 1$ to n , n is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t .

R_i = Amplitude of p_{th} term.

τ_i = Time constant of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i , K/W	0.00007989	0.002973	0.0005936	0.000846	0.00005975	0.003948
τ_{ij} , S	1.688	0.06219	0.002329	0.138	0.0003243	0.9533

DC Anode side cooled

i	1	2	3	4	5	6
R_i , K/W	0.01013	0.004062	0.0009401	0.002853	0.0005963	0.00005641
τ_{ij} , S	9.747	1.058	0.1304	0.06179	0.002313	0.0003013

DC Cathode side cooled

i	1	2	3	4	5	6
R_i , K/W	0.006619	0.004034	0.0008595	0.002956	0.0005965	0.00005689
τ_{ij} , S	9.744	1.025	0.1394	0.06237	0.002318	0.0003037

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

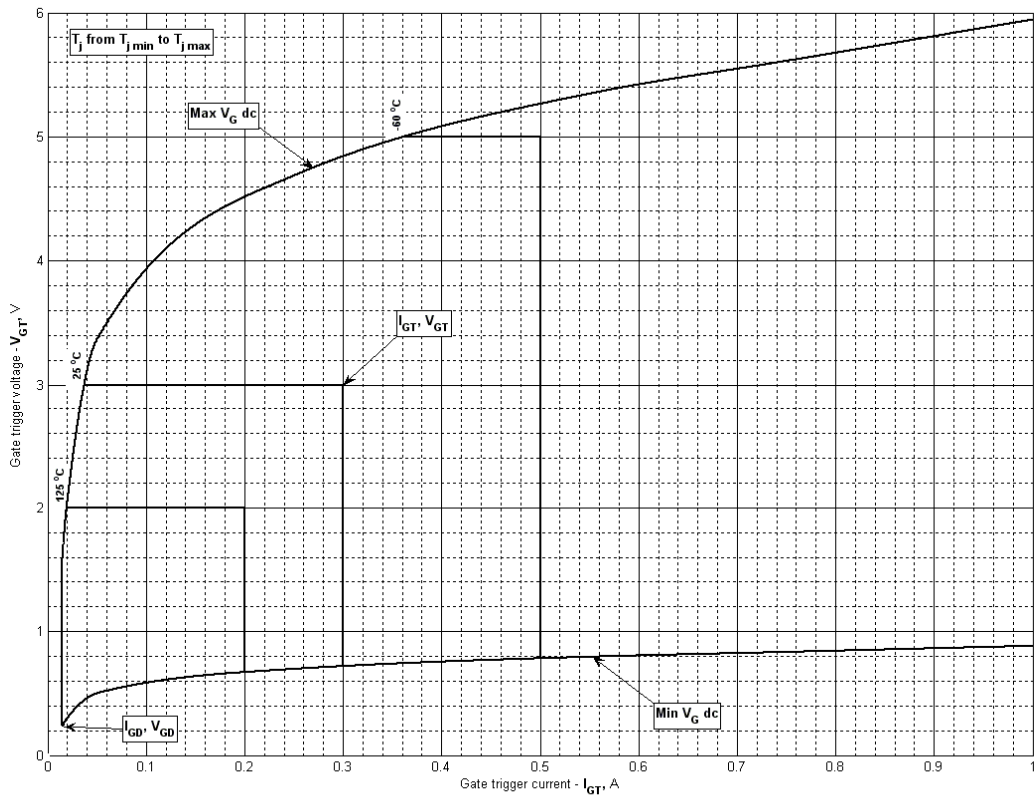


Fig 3 – Gate characteristics – Trigger limits

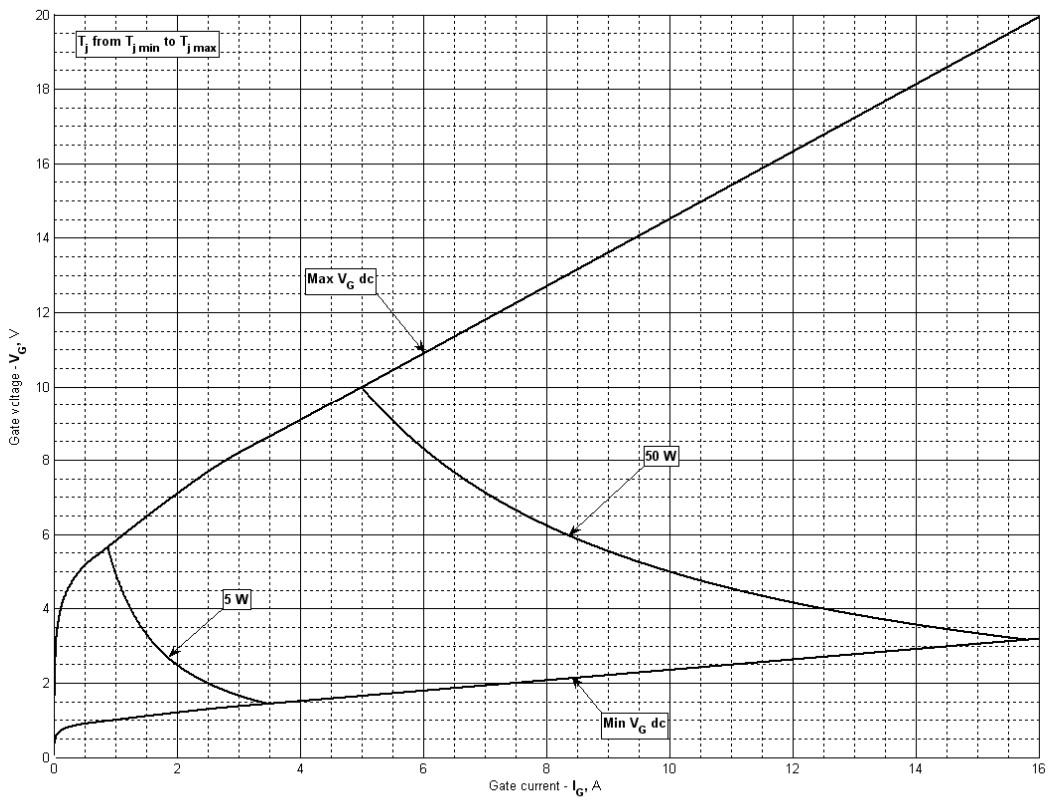


Fig 4 - Gate characteristics – Power curves

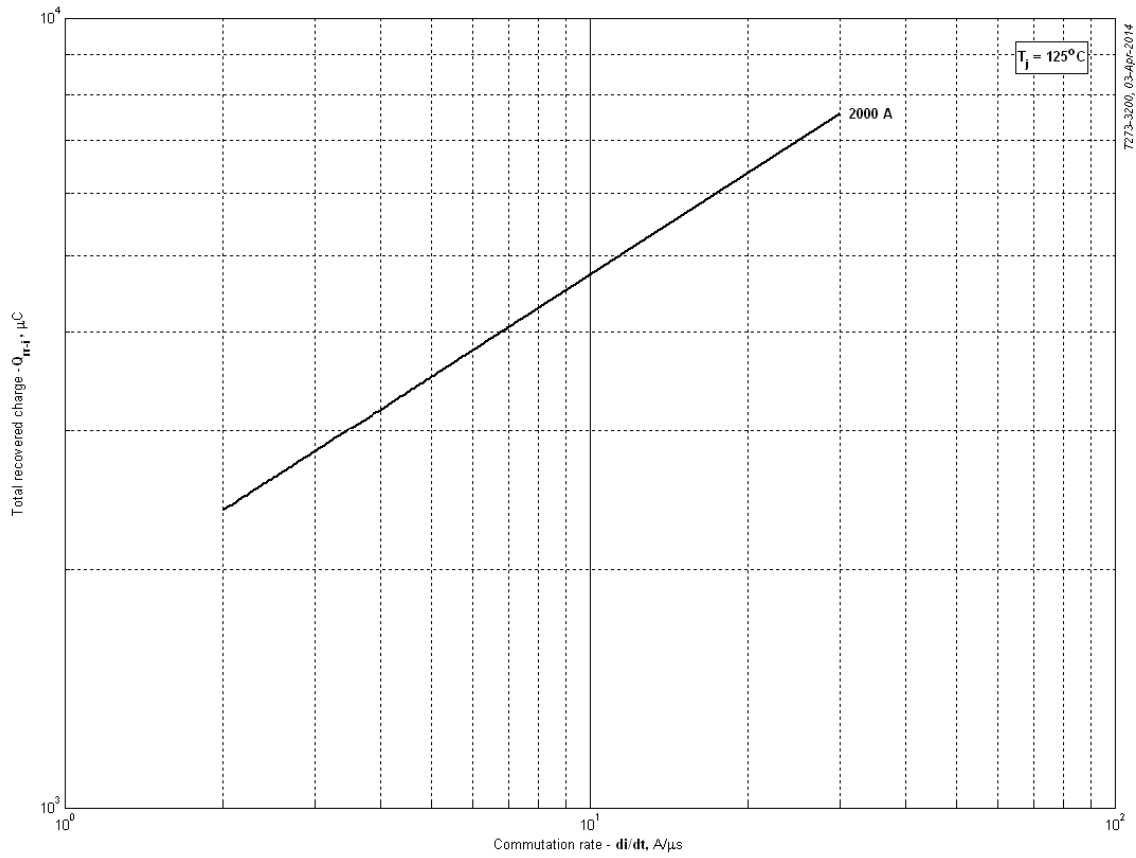


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

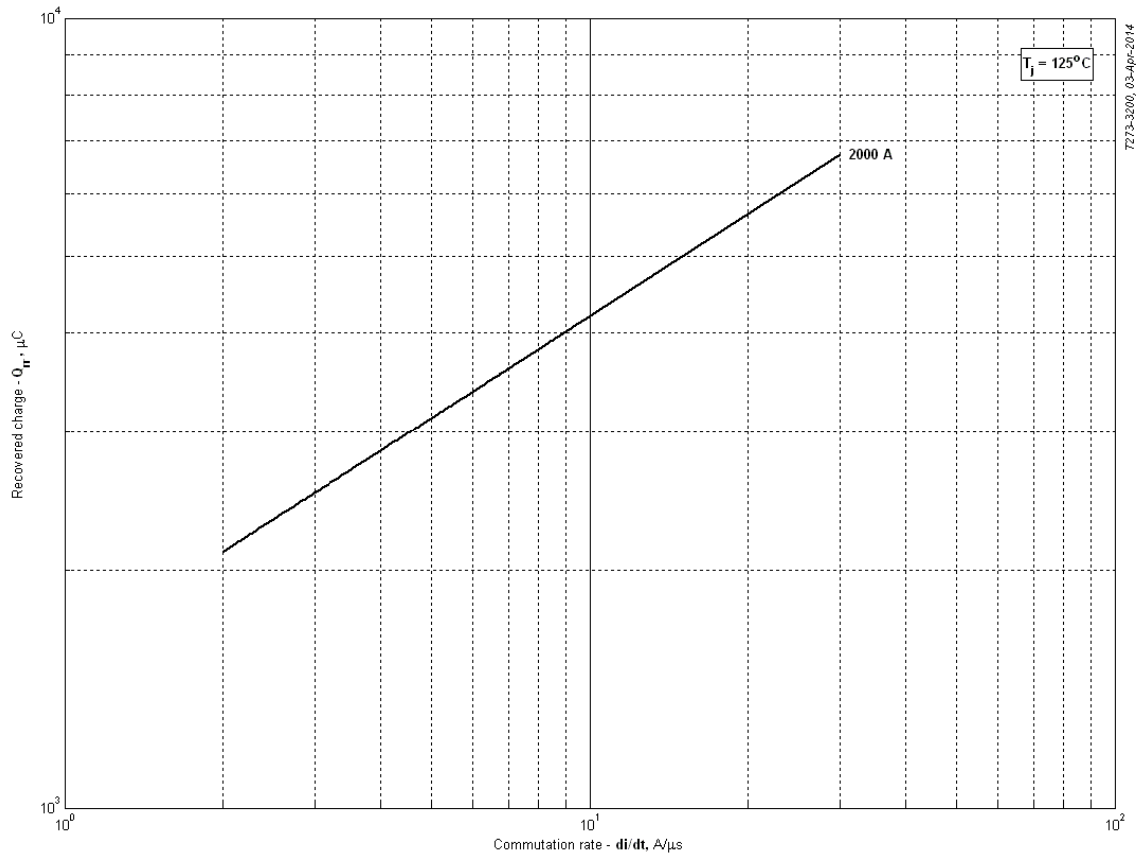


Fig 6 - Recovered charge, Q_{rr} (linear)

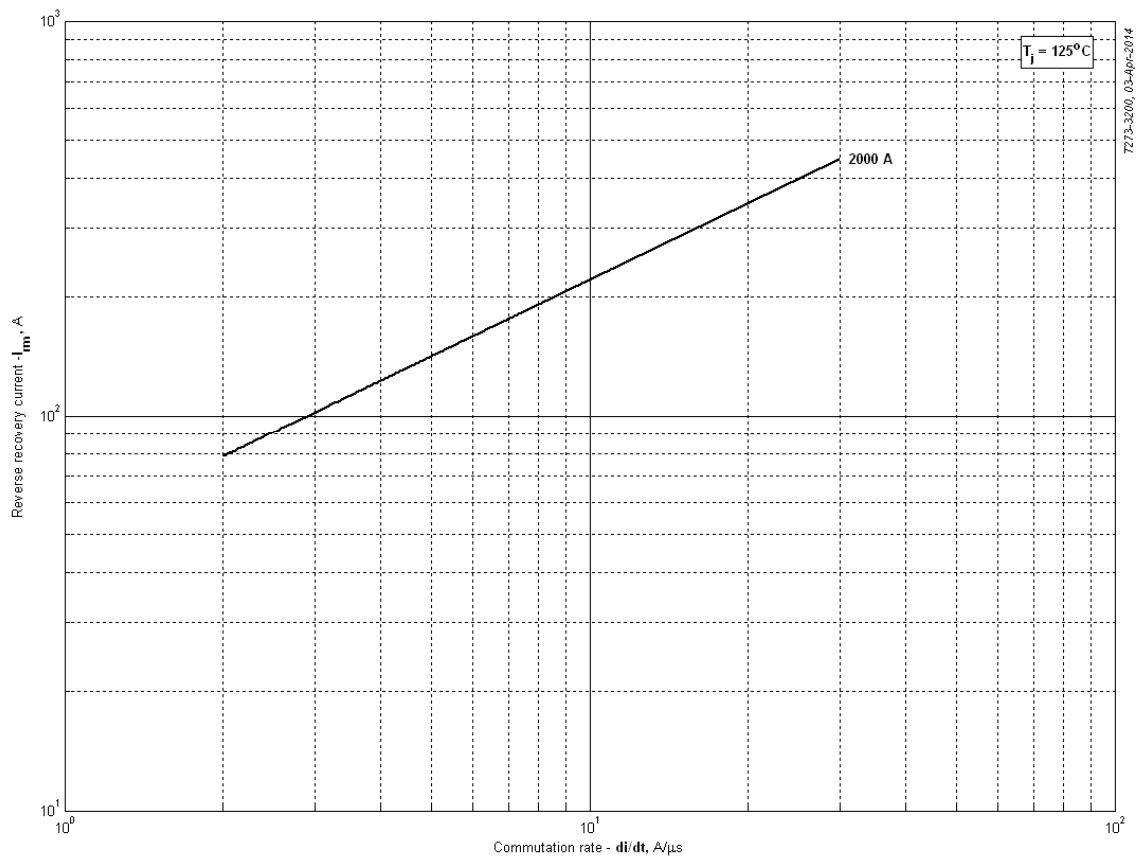


Fig 7 – Peak reverse recovery current, I_{rm}

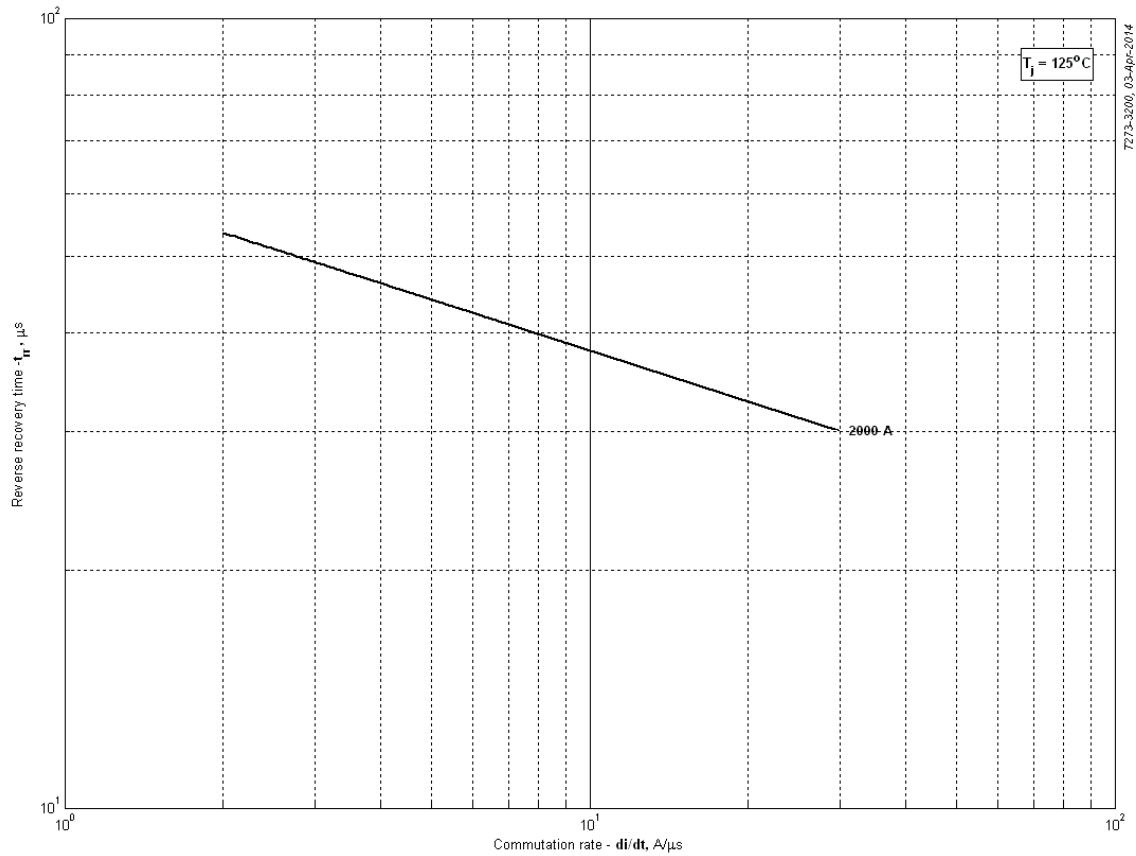


Fig 8 – Maximum recovery time, t_{rr} (linear)

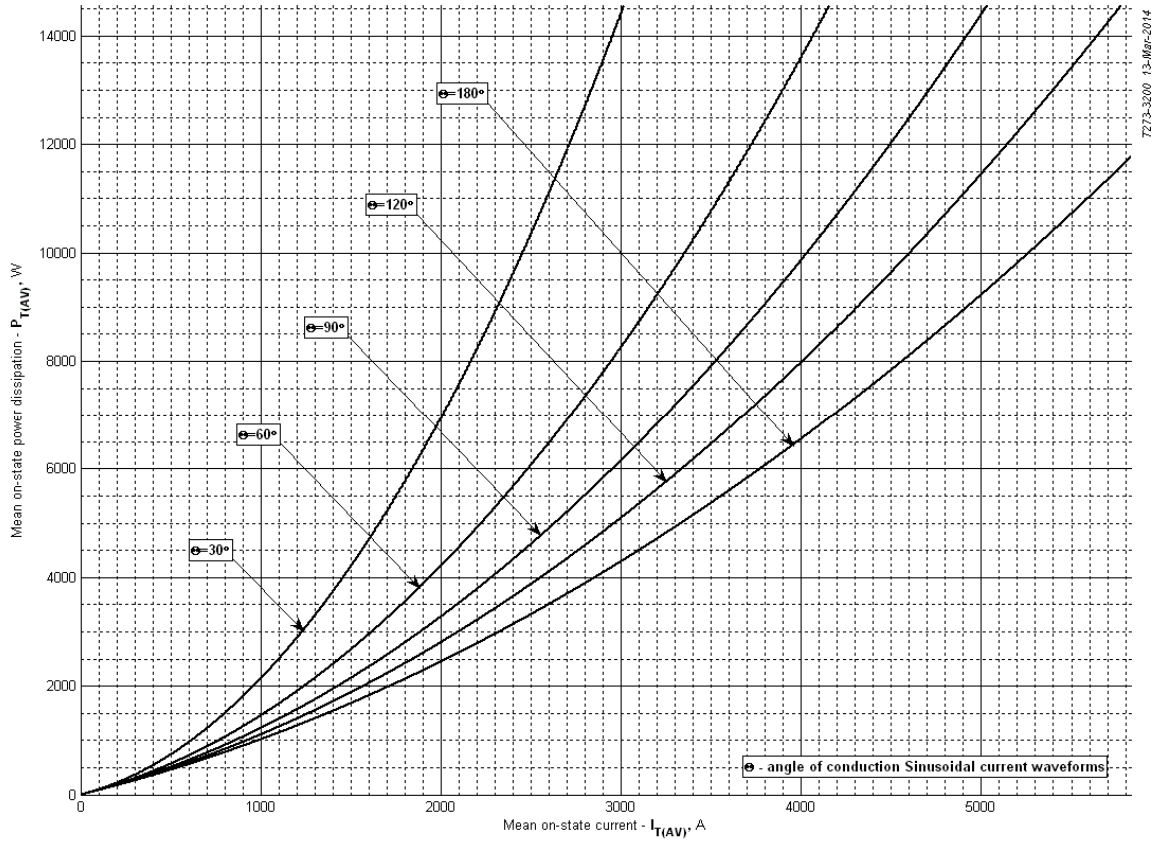


Fig 9 – On-state power loss (sinusoidal current waveforms)

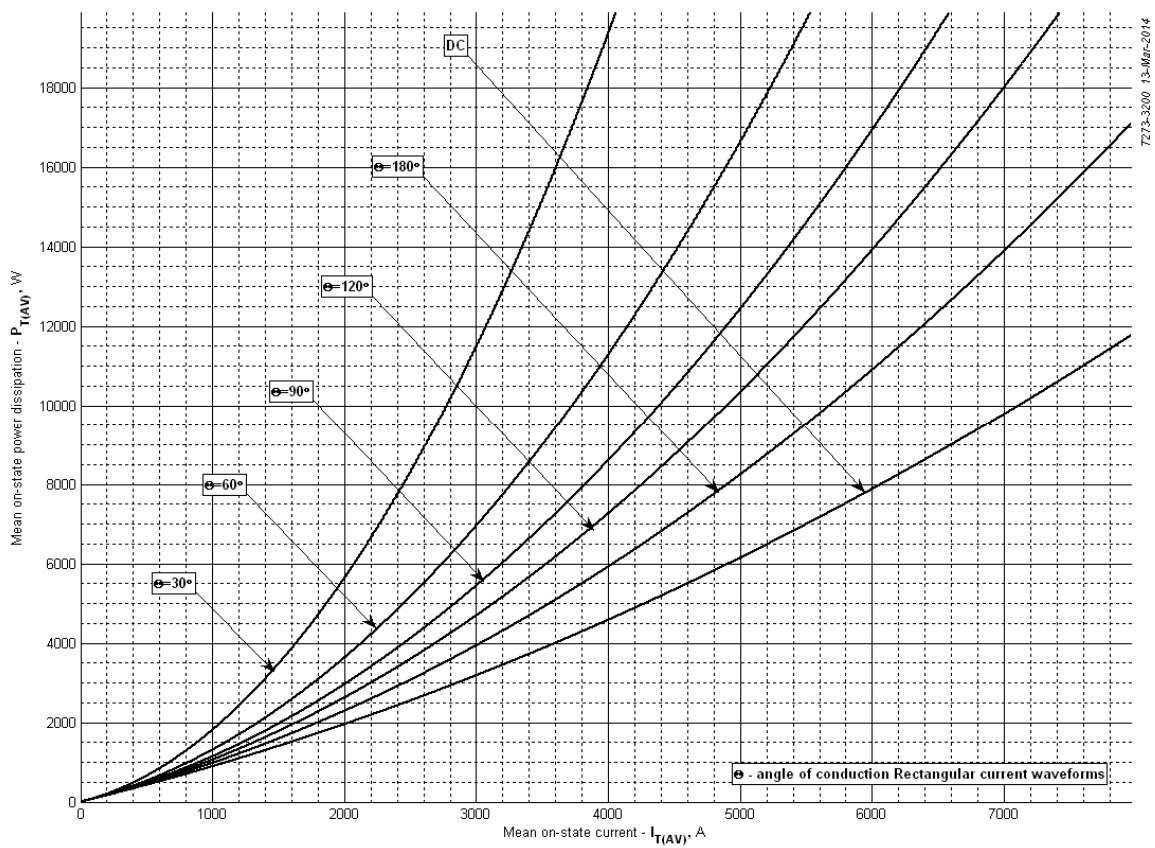


Fig 10 – On-state power loss (rectangular current waveforms)

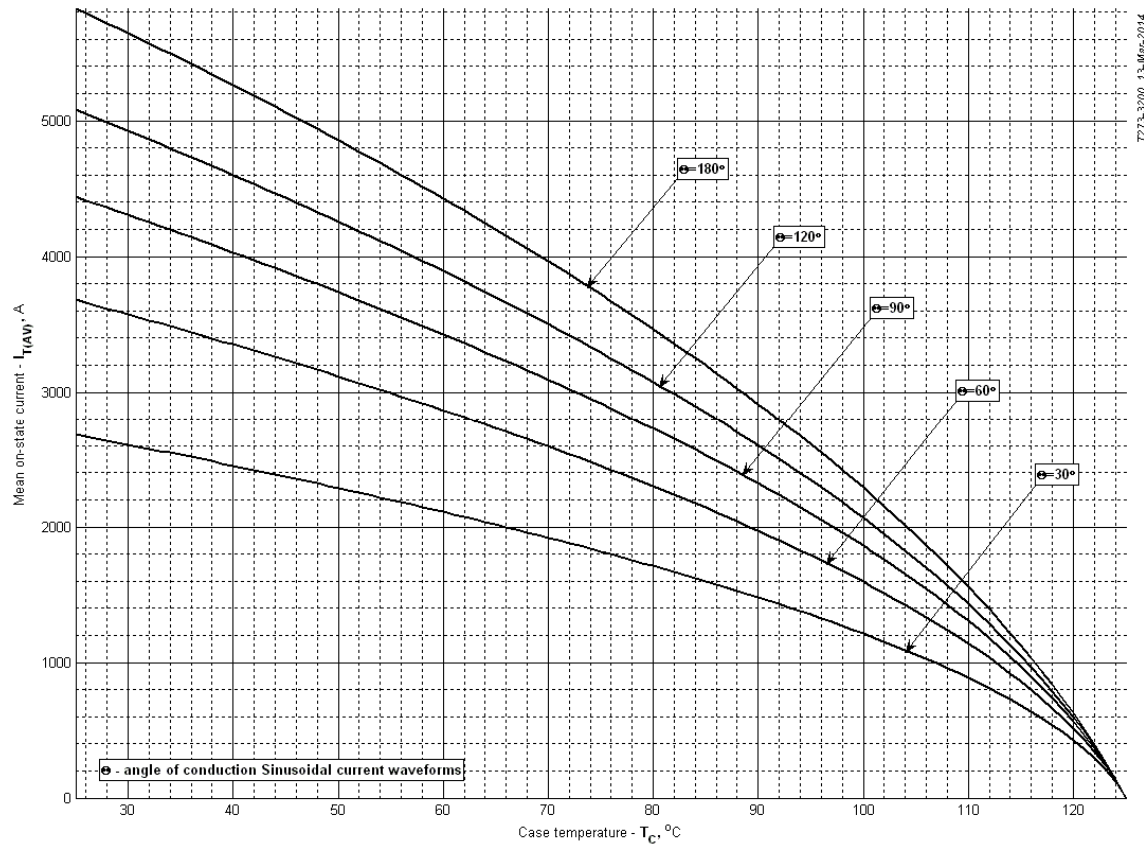


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

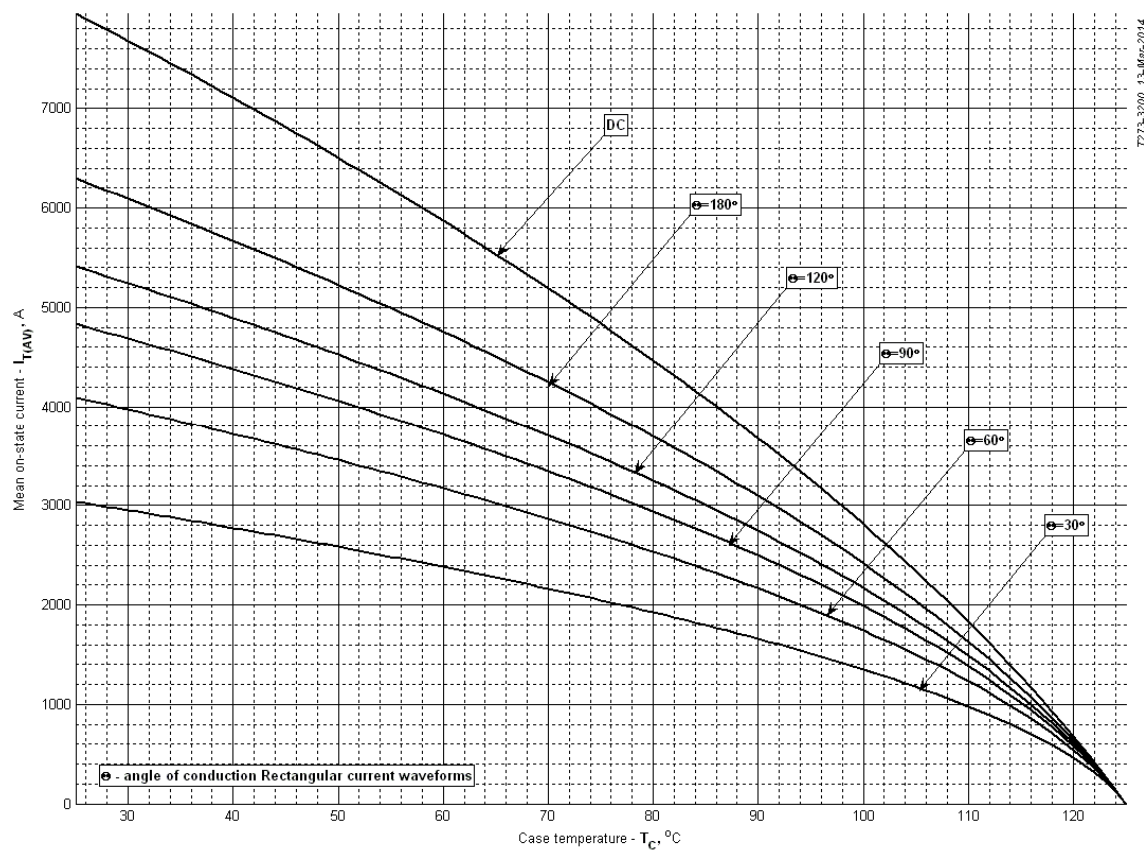


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

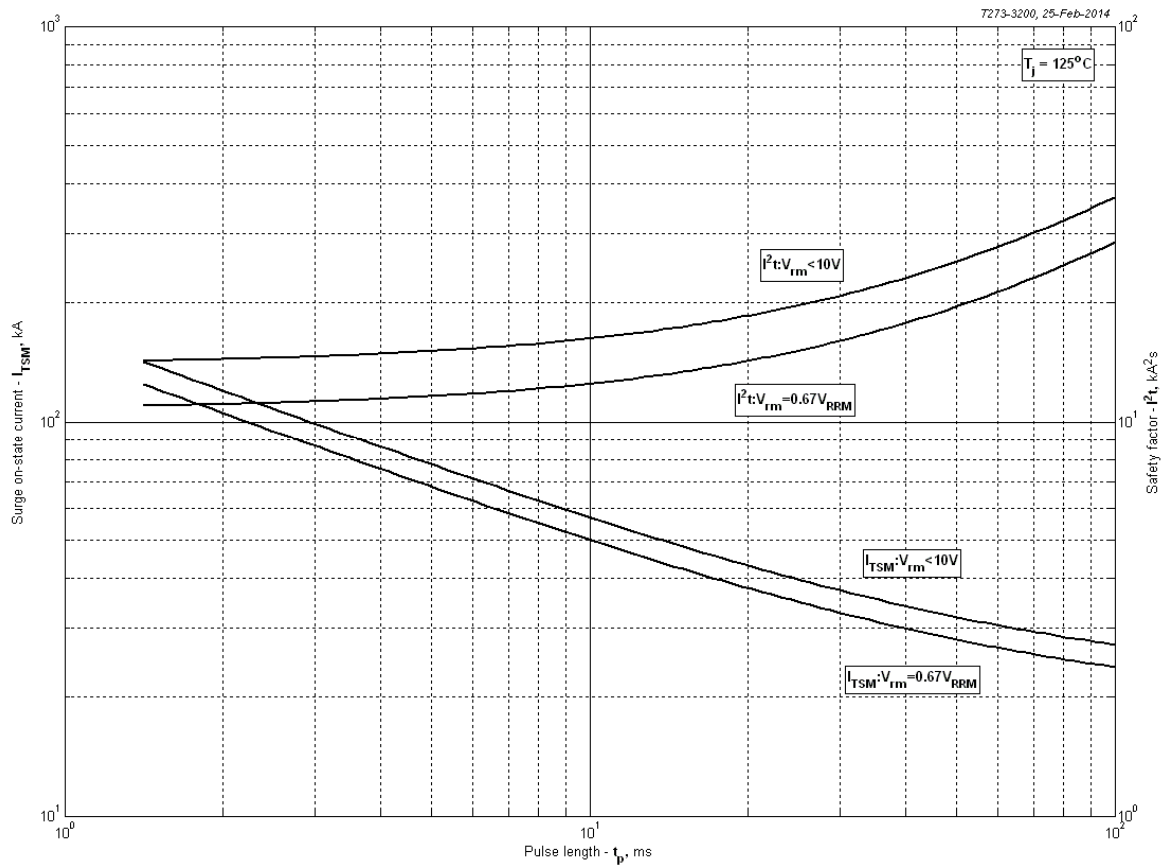


Fig 13 – Maximum surge and I^2t ratings

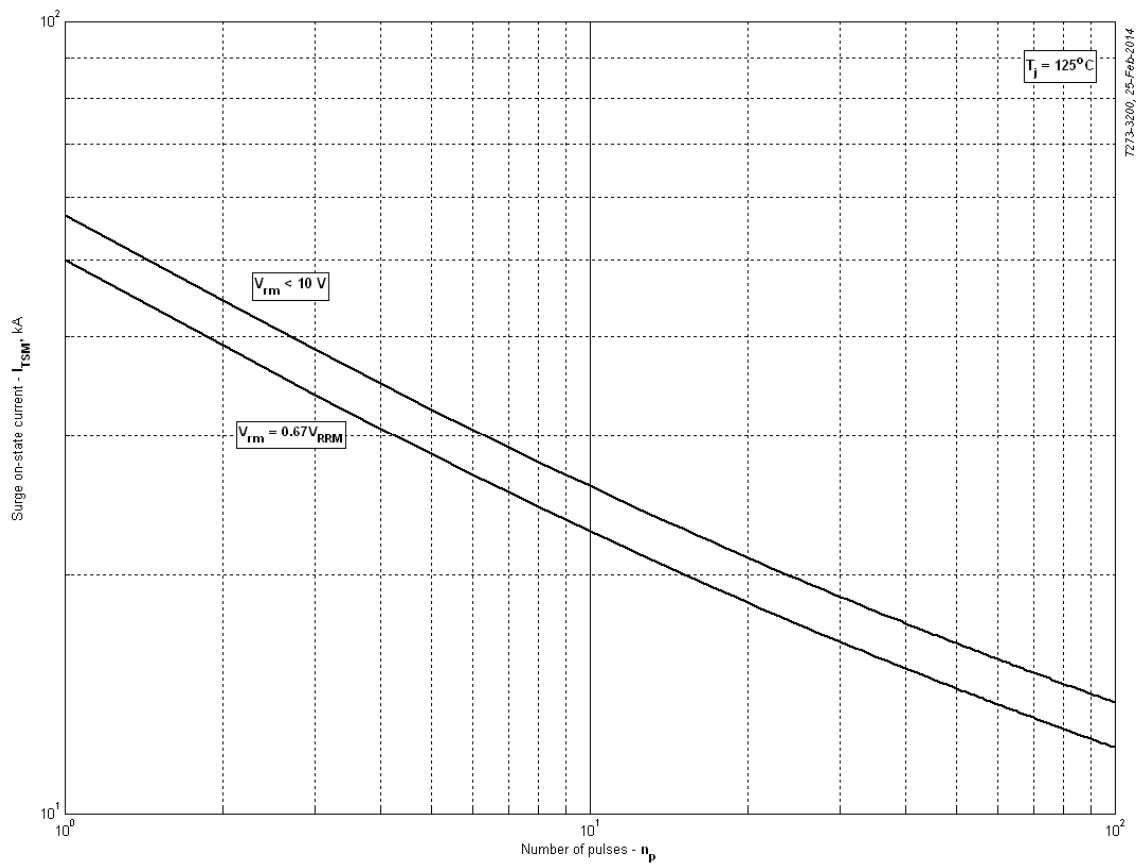


Fig 14 – Maximum surge ratings