



High power cycling capability  
Low on-state and switching losses  
Designed for traction and industrial applications

## Phase Control Thyristor Type T333-400-24

Mean on-state current	$I_{TAV}$	400 A	
Repetitive peak off-state voltage	$V_{DRM}$	2000 ÷ 2400 V	
Repetitive peak reverse voltage	$V_{RRM}$		
Turn-off time	$t_q$	200 $\mu$ s	
$V_{DRM}, V_{RRM}, V$	2000	2200	2400
Voltage code	20	22	24
$T_j, ^\circ C$	-60 ÷ 125		

### MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
<b>ON-STATE</b>				
$I_{TAV}$	Mean on-state current	A	400 415	$T_c=87^\circ C$ , Double side cooled $T_c=85^\circ C$ , Double side cooled 180° half-sine wave; 50 Hz
$I_{TRMS}$	RMS on-state current	A	628	$T_c=87^\circ C$ , Double side cooled 180° half-sine wave; 50 Hz
$I_{TSM}$	Surge on-state current	kA	7.0 8.1	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ( $t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
			8.0 9.2	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ( $t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
$I^2t$	Safety factor	$A^2s \cdot 10^3$	245 325	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 50 Hz ( $t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
			265 350	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave; 60 Hz ( $t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
<b>BLOCKING</b>				
$V_{DRM}, V_{RRM}$	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000 ÷ 2400	$T_{j\ min} < T_j < T_{j\ max}$ ; 180° half-sine wave; 50 Hz; Gate open
$V_{DSM}, V_{RSM}$	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100 ÷ 2500	$T_{j\ min} < T_j < T_{j\ max}$ ; 180° half-sine wave; 50 Hz; single pulse; Gate open
$V_D, V_R$	Direct off-state and Direct reverse voltages	V	$0.75 \cdot V_{DRM}$ $0.75 \cdot V_{RRM}$	$T_j=T_{j\ max}$ ; Gate open

<b>TRIGGERING</b>				
$I_{FGM}$	Peak forward gate current	A	6	$T_j = T_{j\ max}$
$V_{RGM}$	Peak reverse gate voltage	V	5	
$P_G$	Gate power dissipation	W	3	$T_j = T_{j\ max}$ for DC gate current
<b>SWITCHING</b>				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ $\mu$ s	320	$T_j = T_{j\ max}; V_D = 0.67 \cdot V_{DRM}; I_{TM} = 2 I_{TAV};$ Gate pulse: $I_G = 2\ A;$ $t_{GP} = 50\ \mu s; di_G/dt \geq 1\ A/\mu s$
<b>THERMAL</b>				
$T_{stg}$	Storage temperature	$^{\circ}C$	-60 ÷ 125	
$T_j$	Operating junction temperature	$^{\circ}C$	-60 ÷ 125	
<b>MECHANICAL</b>				
F	Mounting force	kN	9.0 ÷ 11.0	
a	Acceleration	$m/s^2$	50 100	Device unclamped Device clamped

## CHARACTERISTICS

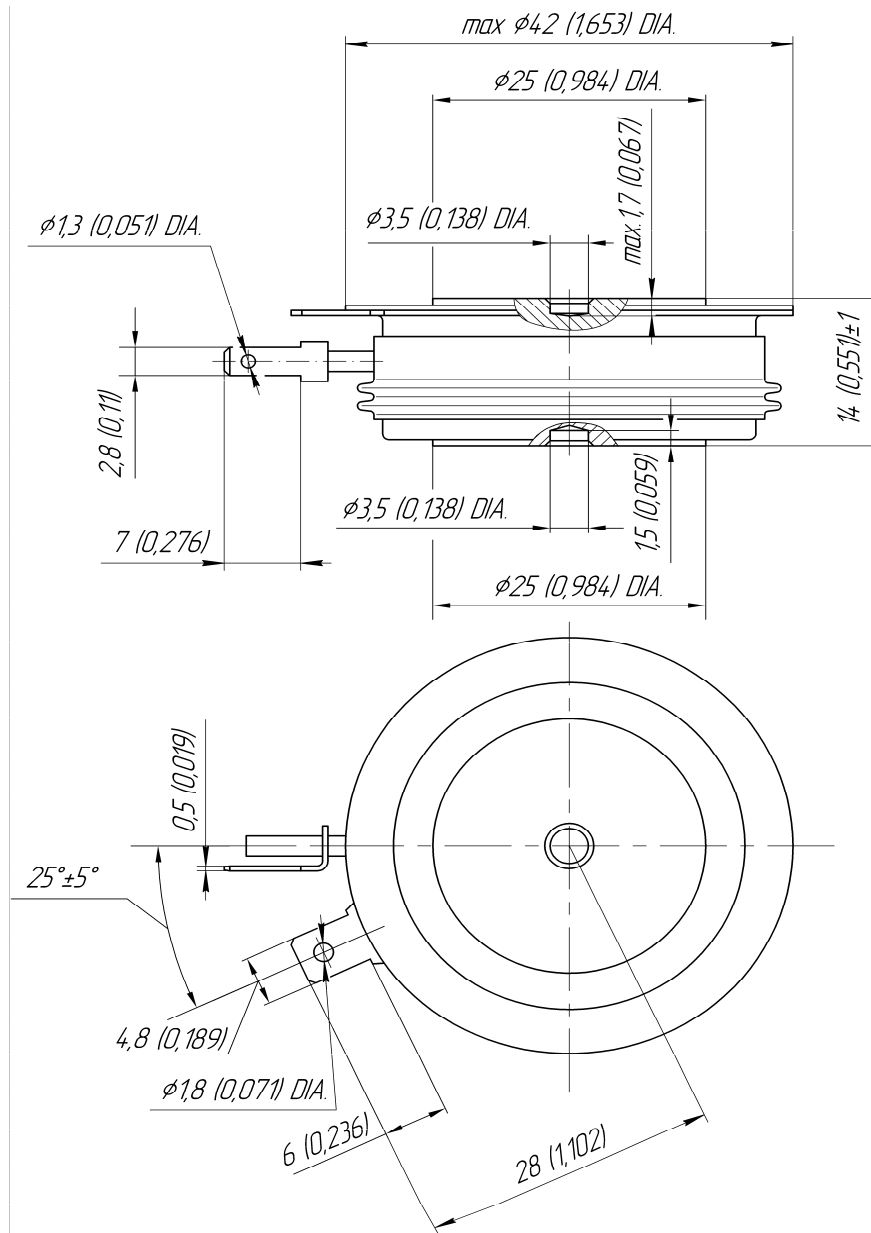
Symbols and parameters		Units	Values	Conditions	
<b>ON-STATE</b>					
$V_{TM}$	Peak on-state voltage, max	V	2.10	$T_j = 25\ ^{\circ}C; I_{TM} = 1256\ A$	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	$T_j = T_{j\ max};$	
$r_T$	On-state slope resistance, max	m $\Omega$	1.250	$0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
$I_L$	Latching current, max	mA	700	$T_j = 25\ ^{\circ}C; V_D = 12\ V;$ Gate pulse: $I_G = 2\ A;$ $t_{GP} = 50\ \mu s; di_G/dt \geq 1\ A/\mu s$	
$I_H$	Holding current, max	mA	300	$T_j = 25\ ^{\circ}C;$ $V_D = 12\ V; \text{ Gate open}$	
<b>BLOCKING</b>					
$I_{DRM}, I_{RRM}$	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j = T_{j\ max};$ $V_D = V_{DRM}; V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage <sup>1)</sup> , min	V/ $\mu$ s	1000	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM}; \text{ Gate open}$	
<b>TRIGGERING</b>					
$V_{GT}$	Gate trigger direct voltage, max	V	4.00	$T_j = T_{j\ min}$ $T_j = 25\ ^{\circ}C$	$V_D = 12\ V; I_D = 3\ A;$ Direct gate current
			2.50		
$I_{GT}$	Gate trigger direct current, max	mA	400	$T_j = T_{j\ min}$ $T_j = 25\ ^{\circ}C$	
			250		
$V_{GD}$	Gate non-trigger direct voltage, min	V	0.25	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$	
			$I_{GD}$		Gate non-trigger direct current, min
<b>SWITCHING</b>					
$t_{gd}$	Delay time	$\mu$ s	2.50	$T_j = 25\ ^{\circ}C; V_D = 0.4 \cdot V_{DRM}; I_{TM} = I_{TAV};$ Gate pulse: $I_G = 2\ A;$ $t_{GP} = 50\ \mu s; di_G/dt \geq 1\ A/\mu s$	
$t_q$	Turn-off time <sup>2)</sup> , max	$\mu$ s	200	$dv_D/dt = 50\ V/\mu s; T_j = T_{j\ max}; I_{TM} = I_{TAV};$ $di_R/dt = -10\ A/\mu s; V_R = 100V;$ $V_D = 0.67 \cdot V_{DRM}$	

<b>THERMAL</b>					
$R_{thjc}$	Thermal resistance, junction to case, max	°C/W	0.040	Direct current	Double side cooled
$R_{thjc-A}$			0.088		Anode side cooled
$R_{thjc-K}$			0.072		Cathode side cooled
$R_{thck}$	Thermal resistance, case to heatsink, max	°C/W	0.008	Direct current	
<b>MECHANICAL</b>					
w	Weight, typ	g	110		
$D_s$	Surface creepage distance	mm (inch)	10.30 (0.405)		
$D_a$	Air strike distance	mm (inch)	6.30 (0.248)		

### **PART NUMBERING GUIDE**

T	333	400	24	N
1	2	3	4	5

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Ambient conditions: N – normal; T – tropical



All dimensions in millimeters (inches)