



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T193-4000-28

Mean on-state current	I_{TAV}	4000 A			
Repetitive peak off-state voltage	V_{DRM}	2000 ÷ 2800 V			
Repetitive peak reverse voltage	V_{RRM}				
Turn-off time	t_q	500 μ s			
V_{DRM}, V_{RRM}, V	2000	2200	2400	2600	2800
Voltage code	20	22	24	26	28
$T_j, ^\circ C$	- 60 ÷ 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	4000 5420	$T_c = 90^\circ C$, Double side cooled $T_c = 70^\circ C$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	6280	$T_c = 90^\circ C$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	75.0 86.0	$T_j = T_{jmax}$ $T_j = 25^\circ C$	180° half-sine wave; 50 Hz ($t_p = 10$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
			79.0 91.0	$T_j = T_{jmax}$ $T_j = 25^\circ C$	180° half-sine wave; 60 Hz ($t_p = 8.3$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	28125 36980	$T_j = T_{jmax}$ $T_j = 25^\circ C$	180° half-sine wave; 50 Hz ($t_p = 10$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
			25900 34365	$T_j = T_{jmax}$ $T_j = 25^\circ C$	180° half-sine wave; 60 Hz ($t_p = 8.3$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000÷2800	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100÷2900	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75 \cdot V_{DRM}$ $0.75 \cdot V_{RRM}$	$T_j = T_{jmax}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	12	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	1000	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2 I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 ÷ 125	
T_j	Operating junction temperature	$^{\circ}$ C	-60 ÷ 125	
MECHANICAL				
F	Mounting force	kN	70.0 ÷ 90.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

CHARACTERISTICS

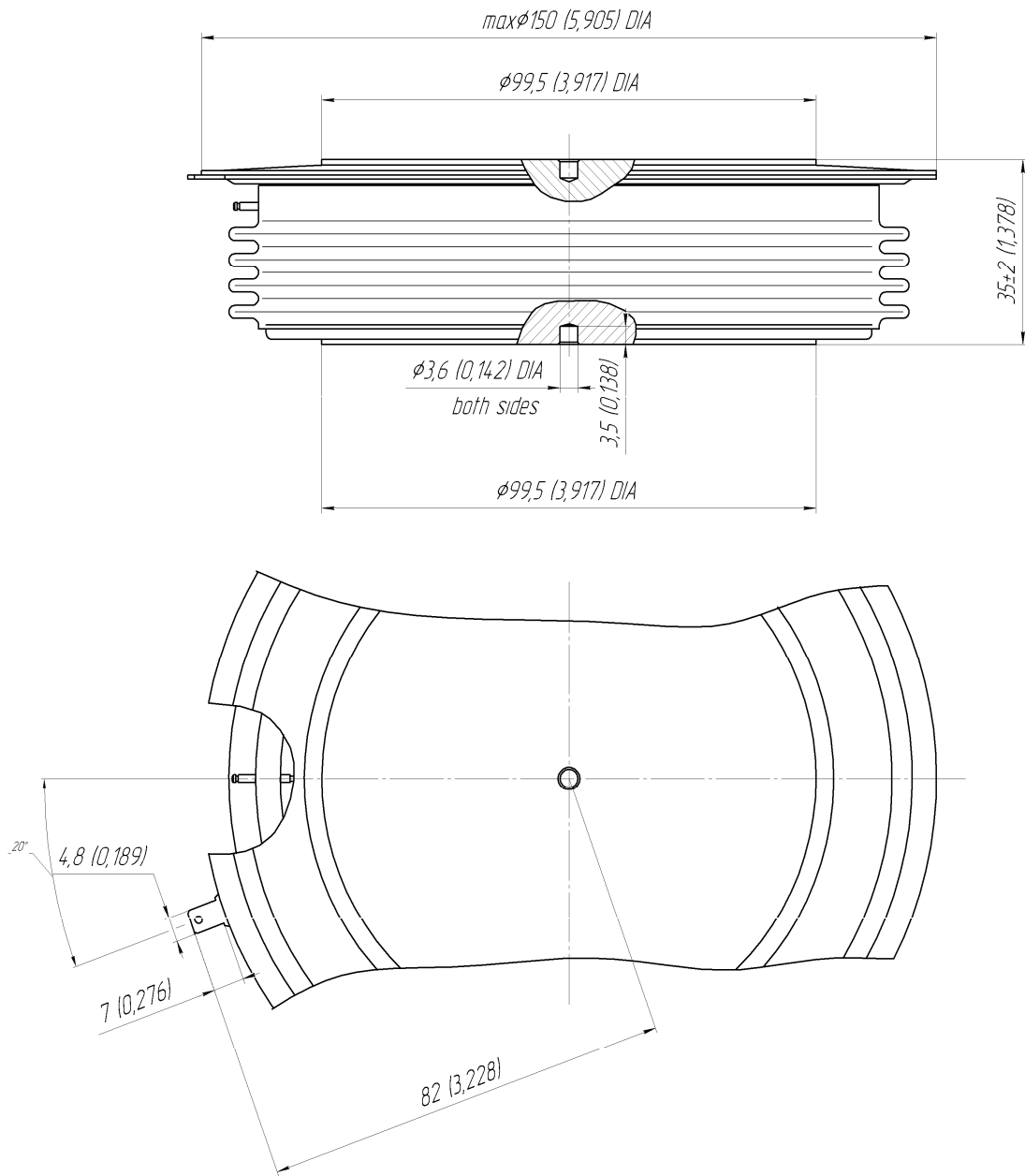
Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.90 1.30	$T_j = 25 \text{ }^{\circ}$ C; $I_{TM} = 8800$ A $T_j = 125 \text{ }^{\circ}$ C; $I_{TM} = 6000$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.85	$T_j = T_{j\ max}$; $0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
r_T	On-state slope resistance, max	m Ω	0.070		
I_L	Latching current, max	mA	1500	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM} , I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j = T_{j\ max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	1000	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00 3.00 2.00	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}$ C $T_j = T_{j\ max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j = T_{j\ min}$ $T_j = 25 \text{ }^{\circ}$ C $T_j = T_{j\ max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	15.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	2.50	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 0.4 \cdot V_{DRM}$; $I_{TM} = 2000$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	500	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}$; $I_{TM} = 2000$ A; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 V_{DRM}$;	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0057	Direct current	Double side cooled
R_{thjc-A}			0.0125		Anode side cooled
R_{thjc-K}			0.0103		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0010	Direct current	
MECHANICAL					
w	Weight, typ	g	2700		
D_s	Surface creepage distance	mm (inch)	62.16 (2.447)		
D_a	Air strike distance	mm (inch)	26.00 (1.024)		

PART NUMBERING GUIDE

T	193	4000	28	N
1	2	3	4	5

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Ambient conditions: N – normal; T – tropical



All dimensions in millimeters (inches)