



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T133-630-8

Mean on-state current	I_{TAV}		630 A					
Repetitive peak off-state voltage	V_{DRM}		100 ÷ 800 V					
Repetitive peak reverse voltage	V_{RRM}							
Turn-off time	t_q		125 μ s					
V_{DRM}, V_{RRM}, V	100	200	300	400	500	600	700	800
Voltage code	1	2	3	4	5	6	7	8
$T_j, ^\circ C$	-60 ÷ 150							

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	630 995	$T_c=116^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	989	$T_c=116^\circ C$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	12.0 14.0	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50 \mu s$; $di_G/dt \geq 1$ A/ μs
			13.0 15.0	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50 \mu s$; $di_G/dt \geq 1$ A/ μs
I^2t	Safety factor	$A^2s \cdot 10^3$	720 980	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50 \mu s$; $di_G/dt \geq 1$ A/ μs
			700 930	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50 \mu s$; $di_G/dt \geq 1$ A/ μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	100 ÷ 800	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	200 ÷ 900	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75 \cdot V_{DRM}$ $0.75 \cdot V_{RRM}$	$T_j=T_{jmax}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	320	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2 I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 ÷ 150	
T_j	Operating junction temperature	$^{\circ}$ C	-60 ÷ 150	
MECHANICAL				
F	Mounting force	kN	9.0 ÷ 11.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

CHARACTERISTICS

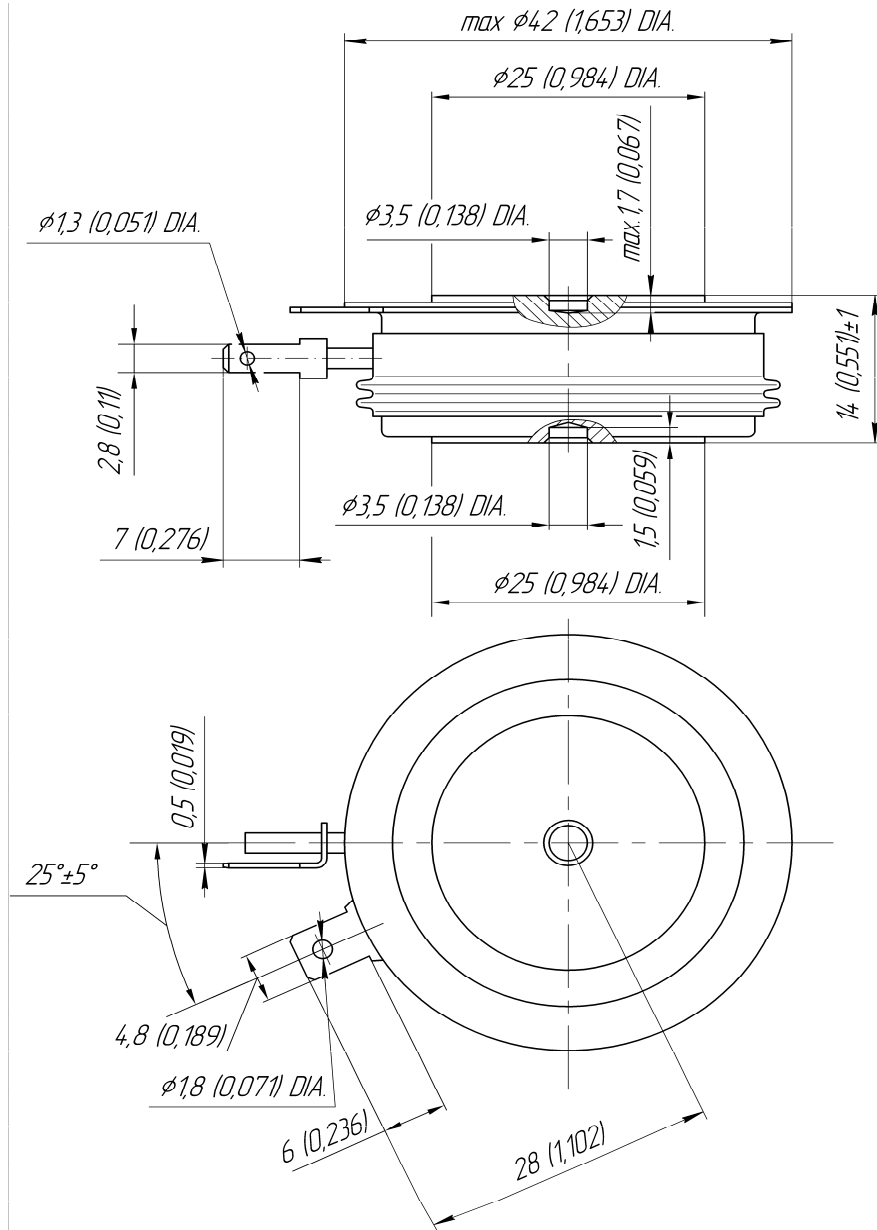
Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.45	$T_j = 25 \text{ }^{\circ}$ C; $I_{TM} = 1978$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.80	$T_j = T_{j\max}$;	
r_T	On-state slope resistance, max	m Ω	0.340	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	700	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM} , I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j = T_{j\max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	1000	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00	$T_j = T_{j\min}$ $T_j = 25 \text{ }^{\circ}$ C $T_j = T_{j\max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			2.50		
			2.00		
I_{GT}	Gate trigger direct current, max	mA	400	$T_j = T_{j\min}$ $T_j = 25 \text{ }^{\circ}$ C $T_j = T_{j\max}$	
			250		
			200		
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	10.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	1.60	$T_j = 25 \text{ }^{\circ}$ C; $V_D = 0.4 \cdot V_{DRM}$; $I_{TM} = I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	125	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.040	Direct current	Double side cooled
R_{thjc-A}			0.088		Anode side cooled
R_{thjc-K}			0.072		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.008	Direct current	
MECHANICAL					
w	Weight, typ	g	110		
D_s	Surface creepage distance	mm (inch)	10.30 (0.405)		
D_a	Air strike distance	mm (inch)	6.30 (0.248)		

PART NUMBERING GUIDE

T	133	630	8	N
1	2	3	4	5

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Ambient conditions: N – normal; T – tropical



All dimensions in millimeters (inches)